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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,826	02/23/2004	Bunshou Kuramori	031948-8	5452

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NIXON PEABODY, LLP
401 9TH STREET, NW
SUITE 900
WASHINGTON, DC 20004-2128

EXAMINER	
KAPLAN, HAL IRA	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/782,826	KURAMORI, BUNSHOU	
	Examiner	Art Unit	
	Hal I. Kaplan	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11* is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☒ Claim(s) *3-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/23/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The disclosure is objected to because of the following informalities: Page 8, lines 17, 23, and 25 and claim 6 refer to transistor 45 as an NMOS transistor, but it is shown in Figure 1 as a PMOS transistor. Page 12, line 30 contains the phrase "PMOS transistors 49i". It appears this should be "PMOS transistors 50i".

Appropriate correction is required.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "17a" and "17b" have been used to designate both PMOS and NMOS transistors in Figure 4. It appears the NMOS transistors should be "18a" and "18b" (see page 15, lines 1-3).

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: MODb in Figure 6 (see page 18, lines 3-6). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of

an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over the US patent of Mitsuishi (5,886,569) in view of the US patent of Kim (5,305,270).

As to claim 1, Mitsuishi, drawn to a semiconductor integrated circuit device with control circuit for controlling an internal source voltage, discloses an internal power supply circuit comprising: a first voltage detector (2) for receiving an external power supply voltage (VEE) and outputting a first detection signal indicating whether the external power supply voltage (VEE) is higher than a first voltage (see column 5, lines

19-20); a first constant voltage generator (31) for generating a first constant voltage (Vrf) from the external power supply voltage (VEE) (see column 7, lines 50-52); and an internal power supply output unit (32) for generating an internal power supply voltage (Vint) from the external power supply voltage (VEE) according to a first reference voltage (Vrf) and outputting the internal power supply voltage (Vint) (see column 7, lines 52-56). Mitsuishi does not disclose a second constant voltage generator or a voltage switch for selecting one of two constant voltages.

Kim, drawn to an initial setup circuit for charging cell plate, discloses an internal power supply circuit comprising: a first constant voltage generator (16) for generating a first constant voltage (V1) from an external power supply voltage (V_{CC}); a second constant voltage generator (18) for generating a second constant voltage (V2) from the external power supply voltage (V_{CC}), the second constant voltage (V2) differing from the first constant voltage (V1), the first constant voltage generator (16) and the second constant voltage generator (18) having identical circuit topologies; and a voltage switch (20,22) for selecting one of the first constant voltage (V1) and the second constant voltage (V2) responsive to a detection signal, and outputting the selected constant voltage (Vcp) (see column 2, lines 23-36 and 55-65, and column 3, lines 9-13). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the circuit of Mitsuishi, by adding a second constant voltage generator and switching between them via a voltage switch as taught by Kim, in order to enable multiple voltages to be output while minimizing power loss.

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mitsuishi in view of Kim, and further in view of the US patent of Cho et al. (6,870,766).

As to claim 2, Mitsuishi in view of Kim disclose all of the claimed features, as set forth above, except for each of the voltage generators comprising an NMOS transistor in series with a pair of resistors. Cho, drawn to multi-level flash memory with temperature compensation, discloses a voltage generator comprising an NMOS transistor (N22) coupled in series with a pair of resistors (R21,R22) (see column 8, lines 1-5 and 12-16, and Figure 8). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to use the voltage generating circuitry of Cho in the constant voltage generators of Mitsuishi in view of Kim, in order to further increase reliability.

Allowable Subject Matter

9. Claim 11 allowed.

10. Claims 3-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

Claim 3 contains allowable subject matter because none of the prior art of record discloses or suggests connecting the gate to a point between the pair of resistors, and obtaining the constant voltage from the drain, in combination with the remaining claimed features.

Claim 4 contains allowable subject matter because, although the prior art of record does disclose a voltage switch comprising a buffer amplifier and two transmission gates, there is no suggestion or motivation to combine a subcircuit of a memory or decoder with a voltage supply, absent applicant's disclosure.

Claims 5 and 6 contain allowable subject matter because none of the prior art of record discloses or suggests five PMOS transistors connected in the claimed topology, in combination with the remaining claimed features.

Claim 7 contains allowable subject matter because none of the prior art of record discloses or suggests the first voltage detector comprising a reference voltage source, a constant voltage source, an inverter, and two pluralities of transistors connected in the claimed topology, in combination with the remaining claimed features.

Claim 8 contains allowable subject matter because none of the prior art of record discloses or suggests an internal power supply output unit comprising a differential amplifier, a second voltage detector, and three transistors connected in the claimed topology, in combination with the remaining claimed features.

Claims 9-10 contain allowable subject matter because none of the prior art of record discloses or suggests a voltage booster for receiving a clock signal, second and third voltage detectors, and a clock generator, in combination with the remaining claimed features.

12. The following is an examiner's statement of reasons for allowance:

Claim 11 is allowed because none of the prior art of record discloses or suggests

at least one mode detector, a plurality of voltage detectors, a selector, two constant voltage generators, a voltage switch, and an internal power supply output unit, in combination with the remaining claimed features.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The US patent of Huang et al. (6,058,059) discloses a similar voltage switch.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hal I. Kaplan whose telephone number is 571-272-8587. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

hik

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800